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DESIGN OF VERTICALLY INTEGRATED CIRCUITS USING CURRENT 2D DIGITAL DESIGN SOFTWARE

233.01 ” NANO-MICROELECTRONICS AND OPTOELECTRONICS”

Abstract of the doctoral thesis in engineering sciences

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CONCEPTUAL FRAMEWORK OF THE RESEARCH

Relevance and Importance of the Research Topic. The research and development of new design methodologies for monolithic 3D integrated circuits will usher in a new era for Moore's Law in the semiconductor and microelectronics industries, paving the way for continued growth in integration density [1]. A number of studies have investigated monolithic 3D integrated circuits from a theoretical perspective. Davis et al. reported a threefold reduction in total silicon area and a twelvefold reduction in circuit dimensions for a four-tier monolithic 3D integrated circuit compared with its 2D counterpart [2]. The reduction in the length of interconnects used to establish circuit connections enables the use of smaller repeaters, thereby decreasing the distance between logic gates and creating a "positive feedback effect" that leads to a significant reduction in silicon area. Zhou et al. reported an improvement of more than one order of magnitude in the power–area–delay (PAD) product for a low-density parity-check (LDPC) decoder [3].

A study [4] demonstrates that the diameter of through-silicon vias (TSVs), which provide vertical interconnects between silicon layers, has a significant impact on the area, interconnect length, delay, and power consumption of 3D integrated circuits implemented in 45 nm and 22 nm technologies. Furthermore, the study shows that, when the number of TSVs is carefully optimized, a 3D circuit outperforms its equivalent 2D implementation in terms of both interconnect length and propagation delay. For the benchmark circuit considered in the study, TSVs occupy approximately 40% of the total chip area. This large footprint also results in increased interconnect lengths. When TSVs with smaller diameters are employed, the area occupied by TSVs is reduced to only 11.2% for the same benchmark circuit. Consequently, the interconnect length is also reduced, resulting in a critical-path delay approximately 36% lower than that of the equivalent 2D circuit.

Established Electronic Design Automation (EDA) tools (e.g., Synopsys and Cadence) do not yet provide native support for monolithic 3D integration on a single silicon die. However, such functionality is expected to be incorporated into future generations of EDA tools. One of the objectives of this dissertation is to integrate the proposed methodologies into existing EDA tools and to validate the practical feasibility of the proposed design flow.

Innovative design and automation techniques are essential for the successful implementation of 3D integration. In particular, partitioning has a significant impact on circuit performance across all levels of abstraction. Moreover, optimizations performed at higher levels of abstraction can yield greater benefits than those achieved at lower levels. Consequently, functional partitioning at the architectural level offers greater advantages than circuit partitioning

at the physical level, as it optimizes the functionality–connectivity relationships among logic blocks. Furthermore, the challenges associated with architectural-level partitioning [5] are generally less complex than those encountered during physical-level partitioning, involving tens or hundreds of logic blocks rather than millions or billions of logic cells.

The problem of functional partitioning is not a recent topic of interest in the field of integrated circuit design. Owing to their shorter development cycles and relatively low implementation costs, field-programmable gate arrays (FPGAs) have been widely used as a rapid prototyping platform for application-specific integrated circuits (ASICs). Furthermore, the integration of FPGAs with field-programmable interconnect circuits (FPICs) has led to the emergence of reconfigurable hardware architectures, which have become an important trend in rapid prototyping and computationally intensive applications. One of the key challenges in multi-FPGA implementations is the optimal partitioning of the circuit across multiple devices [6].

Monolithic 3D integration employs monolithic inter-tier vias (MIVs), which are fine-pitch vertical interconnects used to connect different active layers. Inter-layer vias (ILVs) have dimensions comparable to the minimum feature size achievable through the photolithographic process, and their number within an integrated circuit does not constitute a severe design constraint, unlike through-silicon vias (TSVs) or the number of I/O pins. As a result, monolithic 3D integration provides greater design flexibility by enabling functional, performance, and cost optimizations. The objective of this dissertation is to develop methodologies that make such optimizations practical within the design flow for monolithic 3D integrated circuits.

Objective of the Dissertation: To develop an integrated methodology for the design and experimental validation of monolithic 3D integrated circuits, with a particular emphasis on adapting the design flow, technology files, and conventional 2D implementation tools to support vertical integration.

Research Objectives:

- Investigate the capabilities of EDA tools for 2D ASIC design and identify the design stages, technology files, and standard-cell libraries that can be adapted to support the implementation of monolithic 3D structures.
- Develop a methodology for representing the second active layer by modeling memory blocks as virtual serpentine structures and employing the **CLASS COVER** attribute, thereby enabling the efficient use of conventional 2D EDA tools for monolithic 3D implementations.

- Adapting the main stages of the physical implementation flow, including floorplanning, placement, routing, and physical verification, to support the partitioning of functionalities across two active layers.
- Extend the technology files and standard-cell libraries with parameters and attributes specific to monolithic 3D integration, enabling the representation and implementation of three-dimensional structures within existing 2D ASIC design flows.
- Develop and validate a complete monolithic 3D design flow based on the reuse of the existing 2D ASIC EDA infrastructure, using Synopsys tools and performing a comparative evaluation of 2D and monolithic 3D implementations in terms of silicon area, interconnects, resource utilization, and performance.
- Evaluate a partitioning strategy based on the separation of memory and logic across two active layers, and assess its impact on integration density and the implementation efficiency of monolithic 3D integrated circuits.

Scientific novelty of the research results: consists in the development and validation of a comprehensive design methodology for monolithic 3D integrated circuits using exclusively EDA tools intended for conventional 2D ASIC design flows. The research proposes an original method for representing memory blocks through virtual serpentine structures, with the memories defined in LEF files using the **CLASS COVER** attribute. This approach enables the modeling of the second active layer within 2D design environments and the implementation of logic beneath the memory blocks. A logic–memory partitioning strategy across two active layers was developed and validated, and integrated into a unified monolithic 3D physical implementation flow. Furthermore, the effects of vertical integration on silicon area, interconnects, and the clock distribution network were systematically analyzed, and the feasibility of implementing hardware neural structures compatible with the future development of monolithic 3D-based architectures was demonstrated.

Scientific research problem solved: consists in the development and validation of a methodology that enables the implementation of monolithic 3D integrated circuits using EDA tools originally intended for 2D ASIC design. This is achieved through the modeling of memory blocks as virtual serpentine structures and the adaptation of the physical implementation flow to the requirements of vertical integration, thereby overcoming the absence of a well-established design flow for this emerging technology. The proposed methodology enables the evaluation of various monolithic 3D circuit configurations and provides a practical platform for further research toward the development and optimization of EDA tools with native support for monolithic 3D integration. In addition, the technology files developed as part of this methodology can serve as a foundation for future technology libraries supporting monolithic 3D implementation. By enabling

monolithic 3D design through conventional 2D EDA tools, the proposed methodology facilitates the development of smaller and higher-performance integrated circuits while preserving the use of existing, fully amortized semiconductor manufacturing infrastructure.

Theoretical significance and practical value of the dissertation: The proposed methodology establishes the foundation for the development of a comprehensive design flow for monolithic 3D integrated circuits. The application of this methodology is expected to enable the design of significantly higher-performance integrated circuits for everyday electronic devices while maintaining comparable manufacturing costs and reducing power consumption. By utilizing existing semiconductor fabrication equipment, integrated circuit manufacturers will be able to accelerate the introduction of the next generation of semiconductor devices without requiring major investments in new manufacturing infrastructure. The proposed methodology has broad applicability across numerous domains, including industrial, scientific, medical, research, commercial, and defense applications. For example, monolithic 3D integrated circuits could be employed in advanced defense systems, where enhanced computational performance and energy efficiency may improve operational capabilities. Similarly, they could provide the technological foundation for the development of next-generation medical devices with superior performance. Overall, the proposed methodology for monolithic 3D technology demonstrates considerable potential for practical implementation across a wide range of application areas.

Scientific propositions submitted for defense:

1. A methodology for the implementation of monolithic 3D integrated circuits using EDA tools developed for conventional 2D ASIC design has been developed, demonstrating the feasibility of performing three-dimensional physical implementation without modifying commercial EDA tools through the adaptation of the design flow and technology files.
2. A method for abstracting memory blocks using virtual serpentine structures, defined in LEF files with the **CLASS COVER** attribute, has been developed. This approach enables the representation of the second active layer and the implementation of monolithic 3D architectures within a conventional ASIC design flow.
3. Monolithic 3D integration of logic and memory results in a significant reduction in implementation area, interconnect length, and the number of inserted buffers, thereby improving silicon area utilization and the efficiency of physical implementation compared with conventional 2D ASIC implementations.
4. Optimization of the clock distribution network in a monolithic 3D architecture reduces the resources required for the clock tree, the area occupied by clock cells, and clock skew,

resulting in more efficient clock synchronization and a more uniform clock distribution network.

5. The development and validation of a modular three-dimensional neural architecture, referred to as the **Neuronal Grain**, implemented on an FPGA and evaluated using a complete ASIC design flow, demonstrate its feasibility as a fundamental building block for hardware accelerators dedicated to artificial intelligence applications based on monolithic 3D integration.

Presentation of the doctoral dissertation research results.

The principal results of the doctoral dissertation were presented and discussed at:

- *IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S 2015),* New Jersey, USA, 2015.
- *International Conference on Telecommunications, Electronics and Informatics,* Chișinău, Republic of Moldova, 2018.
- *International Conference on Telecommunications, Electronics and Informatics,* Chișinău, Republic of Moldova, 2019.
- *Technical and Scientific Conference of Undergraduate, Master's and Doctoral Students,* Chișinău, Republic of Moldova, 2019.
- *International Conference on Electronics, Communications and Computing (IC ECCO 2024),* Chișinău, Republic of Moldova, 2024.
- *International Symposium on Signals, Circuits, and Systems (ISSCS 2025),* Iași, Romania, 2025.

In addition, Chapter 5 of the dissertation, entitled *Perspectives on the Development of AI Computing Architectures in Monolithic 3D Technology*, was conceived and prepared within the framework of the research project *Regions and (E)DIHs Alliance for AI-at-the-Edge Adoption by European Industry 5.0 Manufacturing SMEs*. This project is funded under the European HORIZON-CL4-2022-TWIN-TRANSITION-01 programme (Project No. 101092069), with the acronym AI REDGIO 5.0. The project website is: https://www.airedgio5-0.eu/.

Publications related to the dissertation. The principal results of the doctoral dissertation have resulted in 10 scientific publications, including 3 SCOPUS-indexed peer-reviewed articles, 1 article published in the *Journal of Engineering Science (JES)*, which is included in the National Register of Scientific Journals, and 1 article published in the *Scientific Bulletin of the Politehnica University of Timișoara*. In addition, the research results have been presented and published in 8

papers at national and international conferences, 3 of which are indexed in the IEEE Xplore Digital Library. The complete list of publications is provided at the end of the dissertation.

The results obtained in the course of this research have been successfully transferred to both industrial and academic environments. In the industrial sector, the proposed methodology has been implemented at Silicon Service SRL, while in academia, the research findings and the content of this dissertation have been incorporated into the teaching materials of the Faculty of Electronics, Telecommunications and Information Technology at the Gheorghe Asachi Technical University of Iași**.** Furthermore, based on the research results, 2 patent applications covering the proposed methodology have been filed with the Romanian State Office for Inventions and Trademarks (OSIM)**.** The documents certifying the industrial and academic implementation, as well as the submission of the patent applications, are provided in the Appendices**.**

Structure of the dissertation: The dissertation consists of an introduction, 5 chapters, general conclusions and recommendations, a bibliography comprising 141 references, and 6 appendices. It contains 113 pages of text, 61 figures, and 5 tables.

Keywords: integrated circuits, nanotechnology, vertical integration, monolithic 3D, EDA.

DISSERTATION CONTENT

The **Introduction** substantiates the relevance of the research topic, describes the current state of the field, defines the aim and objectives of the research, presents the scientific novelty of the research results, the scientific research problem solved, the theoretical significance and practical value of the dissertation, the scientific propositions submitted for defense, the presentation of the research results obtained within the doctoral dissertation, the publications related to the dissertation topic, and a summary of the dissertation chapters.

Chapter 1 presents the current technologies for the implementation of 3D integrated circuits and explains the TSV and monolithic 3D technologies. It provides an overview of the technologies used for integrated circuit implementation in general, as well as the approaches employed for the implementation of 3D integrated circuits. A comparative analysis of the existing 3D implementation technologies is performed, highlighting the advantages and disadvantages of each technology.

Three-dimensional (3D) technology has emerged as a promising solution for improving the performance of integrated circuits while reducing chip area and interconnection length. 3D integration represents a state-of-the-art technology that has undergone significant development in recent years, offering numerous advantages, including enhanced integrated circuit performance, reduced chip area, and lower power consumption.

An intermediate stage between the conventional 2D implementation of integrated circuits and 3D integration was represented by 2.5D integration, which played an important role in the evolution of vertical integration technologies. The increasing demand for higher integrated circuit performance while maintaining reasonable manufacturing costs led first to the development of 2.5D integration and subsequently to full 3D vertical integration. Unlike 3D integration, 2.5D technology does not involve vertical stacking of chips; instead, it refers to a packaging technique in which multiple chips (dies) are placed side by side on a common interposer made of silicon, glass, or organic material. The chips are interconnected through micro-bumps (very small conductive structures) and, in some cases, through TSVs [7] within the interposer, thereby achieving higher performance and integration density than conventional 2D integrated circuits, while avoiding the full complexity associated with 3D stacking.

A three-dimensional (3D) integrated circuit is a configuration in which multiple layers of integrated circuits are vertically interconnected, with the connections established either at the silicon wafer level or at the individual die level. Several techniques for the implementation of three-dimensional integrated circuits are currently available, the most important of which are:

1. Wafer Bonding – In this method, silicon wafers are fabricated and processed individually, after which they are stacked and interconnected using various bonding techniques.
2. Die Stacking – In this method, individual integrated circuits (dies) are separated from the silicon wafer and subsequently stacked and interconnected on an individual basis.
3. A fundamentally different approach is monolithic 3D technology, in which each layer is fabricated directly on top of the previous one on the same silicon wafer, eliminating the need for the subsequent stacking and interconnection of either silicon wafers or individual integrated circuits.

The first two three-dimensional integration methods require high-precision alignment of either silicon wafers or individual integrated circuits (dies), with stacking and interconnection performed after the integrated circuits have been fabricated. In the first method, where the interconnection is established at the silicon wafer level, all dies are processed simultaneously. In contrast, the second method allows each die to be tested individually before stacking, thereby reducing the risk of integrating defective components. Both methods employ through-silicon vias (TSVs) to interconnect the layers. TSVs are vertical interconnects formed by etching holes through the silicon substrate and filling them with a conductive material. At the silicon wafer level, TSVs provide electrical connectivity between multiple layers within a wafer stack, whereas at the die level, they are used to interconnect stacked chips in a three-dimensional architecture. Figure 1 illustrates the interconnection of two individual integrated circuits (2 dies) using TSV technology [8].

Although TSV-based 3D devices have achieved significant progress, the relatively large dimensions of TSVs—typically 3–5 μm in diameter—and the considerable thickness of the stacked layers limit the benefits of this approach. In recent years, an alternative approach (Figure 2) based on the monolithic 3D stacking of semiconductor layers using ultra-thin layers (less than 1 μm thick) has become feasible and promises substantially greater benefits than TSV-based integration. In particular, monolithic inter-tier vias (MIVs) (Figure 2), used in the monolithic 3D integration process [9], are approximately two orders of magnitude smaller than TSVs, enabling much higher vertical interconnect density. This allows the implementation of new system architectures and improves manufacturing yield. Furthermore, the use of ultra-thin layers and the higher interconnect density facilitate more efficient heat dissipation while reducing manufacturing cost.

Monolithic 3D technology is an advanced approach for the fabrication of three-dimensional integrated circuits, in which transistor layers are built sequentially on the same silicon substrate, eliminating the need for stacking and aligning either silicon wafers or individual integrated circuits

as required in TSV-based technology to create three-dimensional integrated circuits. The fabrication process for monolithic 3D integrated circuits begins with a standard silicon substrate on which the first transistor layer is formed. After the first transistor layer and its interconnects have been fabricated, an inter-layer dielectric (ILD) is deposited to electrically isolate it from the subsequent layer. A thin silicon layer is then deposited on top of the ILD using a Low-Temperature Chemical Vapour Deposition (LTCVD) process, forming the substrate for the next transistor layer. The fabrication of the second transistor layer follows the same process as the first, including doping, patterning, and etching. The vertical interconnection between transistor layers is achieved using monolithic inter-tier vias (MIVs), which are comparable in size to the vias employed for metal interconnects in conventional planar 2D technology. An illustration of the dimensions of the MIVs used for vertical interconnection in monolithic 3D technology is shown in Figure 2.

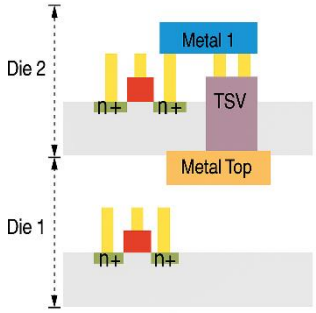


Fig. 1. Interconnection of two individual integrated circuits using TSV technology [8]

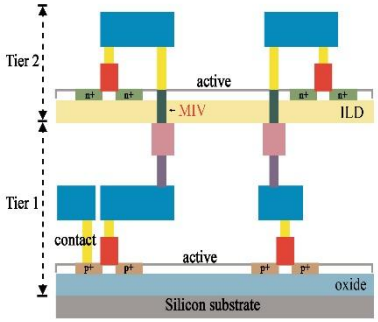


Fig. 2. MIV implemented between two layers in monolithic 3D technology [8]

Monolithic 3D integration technology is a physically demonstrated and technically viable approach; however, it remains predominantly confined to advanced research and experimental laboratory prototypes [10]. Although several implementations have been successfully fabricated and tested to validate the concept, they are still largely limited to academic research and pre-commercial development.

Chapter 2 describes a complete implementation flow for a planar 2D integrated circuit, modelled and optimized using knowledge acquired from the execution of multiple industrial projects in which integrated circuits were successfully manufactured and are currently deployed in commercial applications. The chapter covers all stages of the integrated circuit design and implementation process. Each step required to produce an optimized integrated circuit is presented systematically, beginning with the functional description of the circuit using a hardware description language (HDL), followed by logic synthesis, functional verification, design-for-testability (DFT) preparation, placement, clock tree synthesis (CTS), routing, and finally the generation of the manufacturing database, together with the technological specifications required

for the fabrication process.

Chapter 3 addresses the partitioning of integrated circuits, a critical stage in the transition from conventional 2D integrated circuit design to 3D integration. During the partitioning process, the allocation of components—including both standard cells and memory blocks—to each layer is determined in such a way that the number of vertical interconnections (MIVs or TSVs, depending on the implementation technology) is minimized. The more efficient the partitioning, the fewer vertical interconnections are required, resulting in lower power consumption, reduced signal path delays, and a less complex routing process.

The integration of the partitioning algorithm into the integrated circuit implementation flow is essential for achieving optimal performance, power efficiency, and three-dimensional scalability [11]. Traditionally, the partitioner is introduced immediately after logic synthesis, at a stage where the netlist has already been generated but has not yet undergone physical placement and routing. This strategic position enables the efficient partitioning of the circuit components into functional groups or clusters, which can subsequently be assigned either to individual layers in a 3D implementation or to local regions in a 2D design. The early integration of the partitioning stage facilitates the optimization of internal interconnections, reduces routing congestion, and minimizes the number of TSVs or MIVs required in 3D architectures, thereby improving thermal dissipation and reducing overall latency.

Chapter 4 presents an original methodology for implementing a three-dimensional (3D) integrated circuit by stacking memory blocks above the standard logic cells of a circuit consisting of 50% memory and 50% logic, using the existing 2D design tools provided by Synopsys. Using this methodology, 3 circuit configurations were implemented, and the advantages of 3D integration over conventional 2D implementation were demonstrated [12–14]. The 3D implementation was achieved by modifying the technology files and adapting the design flow so that the 2D tools allowed memory blocks to be stacked above the standard logic cells without reporting overlap violations [15]. All figures illustrating the physical implementation of the circuit (layout) are screenshots captured from the software used to perform the backend design process of the integrated circuit.

Accordingly, the research on 3D integration was carried out using conventional 2D electronic design automation (EDA) tools by adapting the input technology files to enable the stacking of memory blocks above the associated functional logic. One of the main objectives of 3D integration is to reduce the complexity of interconnections and the associated delays inherent in conventional 2D technology. These limitations are considered to be the primary obstacles to further improving the performance of future generations of integrated circuits. Synopsys Design

Compiler was used for circuit synthesis, while Synopsys IC Compiler was employed for the placement and routing stage. The implementation was based on the 32 nm SAED_EDK32/28 educational technology package provided by Synopsys.

For the implementation of the three-dimensional integration process, a specific circuit was selected (although the methodology can be applied to other architectures and circuits) that includes two main categories of components, which can be distributed approximately equally across two layers:

- More than 30,000 standard logic gates were placed on one layer to implement the logical functions of the circuit.
- Nine memory blocks were placed on a second layer for data storage.

This separation between the standard logic gates and the memory blocks was performed so that the cell area on each layer was distributed uniformly, with each layer occupying approximately 50% of the total area of the 3D integrated circuit. This methodology ensures a balanced distribution of resources and optimizes space utilization within the 3D integration process.

The circuit selected for implementation is a block belonging to the OpenSPARC T2 processor, formerly known as UltraSPARC T2. OpenSPARC T2 is an open-source architecture developed by Sun Microsystems and is a multi-core, multi-threaded processor designed to deliver high performance in server applications [16]. The block selected for the 3D implementation is the LSU (Load Store Unit). Its selection was based on a rigorous post-synthesis analysis performed on all the constituent blocks of the openSPARC T2 processor, as illustrated in Fig. 3. The primary selection criterion was to identify a circuit whose functional logic area was approximately equal to the total area of the memories used in the 3D implementation.

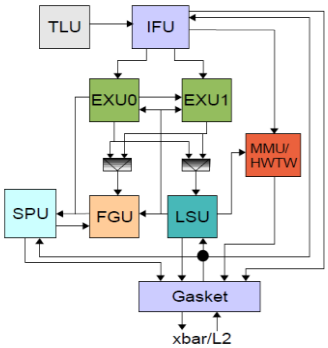


Fig. 3. Diagrama bloc a procesorului openSPARC T2 [16]

The synthesis process of the openSPARC T2 processor's constituent blocks involved evaluating the characteristics of each block in terms of area, complexity, and compatibility with 3D integration.

The memory blocks used in the 3D circuit implementation consist of eight SRAM_128x30slp memory instances and one SRAM_128x38slp memory instance, all generated using the SAED Memory Compiler. The SAED Memory Compiler is a design tool used to generate custom memory macros for specific semiconductor technology nodes, including 90 nm, 45 nm, and 32 nm, based on the Synopsys Academic and Educational Design (SAED**)** technology library. The SAED library is an academic standard-cell and memory library provided by Synopsys for educational purposes and research projects.

After the synthesis stage, the total area of the memory blocks is approximately **180,000 µm²**, while the area occupied by the standard logic cells placed on the first tier is approximately **115,000 µm²**. These values represent preliminary estimates of the silicon area utilized by the design prior to the placement, clock tree synthesis (CTS), optimization, and interconnect routing stages.

The circuit was implemented using a 32 nm CMOS technology provided by Synopsys for educational and research purposes as an open-source educational package. This technology is part of the SAED_EDK32/28nm library, which complies with the design rules of the SAED32/28nm 1P9M 1.05 V/1.8 V/2.4 V process. The technological features of this educational process design kit (PDK) include support for 10 metal layers, ranging from Metal 1 (M1) to the Redistribution Layer (RDL), which serves as the top metal layer. The supported operating conditions include supply voltages of 1.05 V**,** 1.8 V**,** and 2.5 V, as well as operating temperatures of −40 °C**,** 25 °C**,** and 125 °C**.**

The implementation and performance analysis of the circuit were carried out under specific process technology conditions. As in the conventional 2D integration flow, the two process corners representing the most favorable and the most challenging operating conditions were used. By performing timing and power analyses at these two extreme process corners, the correct operation of the circuit is ensured over a wide range of operating conditions, with the entire operating spectrum effectively bounded by these corner cases.

Using the circuit and technology described previously, the initial implementation followed the conventional design flow for a single-tier circuit, corresponding to traditional 2D planar integration. The conventional 2D placement of the circuit, which contains both logic and memory blocks on a single tier, is illustrated in Figure 4. In the first stage, the memory macros were placed, followed by the placement of the logic cells around the memories according to the timing constraints and the interconnections between the circuit components.

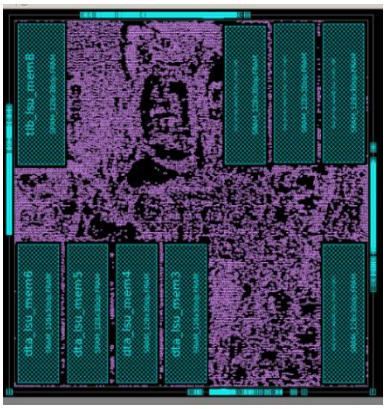


Fig. 4. 2D Placement of Memory Macros and Logic Cells

Both the logic and memory blocks are implemented on the same silicon tier. The selected circuit for implementation consists of approximately 50% memory blocks and 50% logic gates, enabling an efficient utilization of the allocated chip area while clearly highlighting the advantages of three-dimensional (3D) integration**.**

The design flow must be followed step by step to ensure that potential issues are identified and resolved as early as possible, thereby avoiding problems that could otherwise be detected too late to maintain an efficient integrated circuit development process. This design methodology has been extensively validated in conventional 2D planar technology and has been successfully applied in the production of commercial integrated circuits. Failure to identify design issues at the appropriate stages of the implementation flow leads to increased design complexity and longer development cycles. Consequently, the overall design and manufacturing time of an integrated circuit increases in direct proportion to both the number and the severity of the issues identified at later stages of the design process. Through the analysis and refinement of the design flow, the identification of bottlenecks and early-stage design issues, and the adoption of a well-defined implementation methodology, the optimization process ensures a design trajectory with minimal errors, from logic synthesis to the final layout prepared for fabrication. To support this methodology, comprehensive automation scripts were developed for each stage of the physical design flow, including floorplanning**,** power planning**,** placement of standard cells and memory macros**,** clock tree synthesis (CTS)**,** signal routing, and both physical and logical verification**.**

The methodology used for placing the memory blocks above the logic cells in the 3D integration approach consists primarily of the conventional stages of existing 2D integrated circuit design methodologies, complemented by additional steps specifically required for 3D integration. These additional stages address the unique challenges associated with vertically stacked circuit implementation while preserving the well-established and validated principles of the traditional 2D physical design flow.

Using the conventional 2D integrated circuit design flow, the first implementation stage involved placing the memory macros and the input/output (I/O) pins, after which their positions were fixed. For each memory macro on layer 2, a special representation was generated to enable the conventional 2D physical design tool to place logic cells underneath the memory macros. To avoid memory overlap, the separation between the two layers was defined as follows: memory macros on layer 2 and logic cells on layer 1. The generation of the memory representation involved a special serpentine-shaped pattern whose pitch was smaller than the dimensions of the smallest memory macro in the circuit, as shown in Figure 5. The serpentine pattern allows the placement tool to place logic cells underneath the memory macros while preventing the memory macros from overlapping each other. Before adopting this serpentine representation of the memory macros, several letter-shaped representations were evaluated, namely U, L, T, E, F, H, and a spiral ("snail") pattern. However, these representations proved to be less effective because, during the automatic memory placement process, the placement tool allowed, in some cases, the memory macros to overlap.

By using the serpentine representation of the memory macros, the conventional 2D integrated circuit design tool perceives a much smaller area utilization (approximately 1%) than when the memory macros are represented in their actual physical form. This allows the placement of both the memory macros and the logic within 50% of the actual area, where approximately 49% is occupied by the functional logic and 1% by the memory representations.

In the first stage of the backend design flow, referred to as floorplanning, the nine memory macros with special serpentine-shaped representations are placed within the area allocated for the placement of the logic cells and are fixed in their respective locations, as shown in Figure 5. This placement of the memory macros with special serpentine-shaped representations forces the conventional 2D physical design tool to estimate a much smaller area required for the memory macros. As a result, the tool is able to place the logic cells on Layer 1, underneath the memory macros, without reporting overlap violations between the two layers and without indicating an area utilization greater than 100%. During the same floorplanning stage, the circuit I/O pins are also placed along the boundary of the die

In the second stage, the global placement of the logic cells underneath the memory macros was performed according to the timing constraints and the interconnections between the circuit components, as shown in Figure 6. The area utilization for logic placement increases in the case of the 3D circuit integration, owing to the reduced placement area available for the entire logic of

the LSU block. In addition, the interconnect length between components is reduced due to the shorter distances resulting from their vertical arrangement.

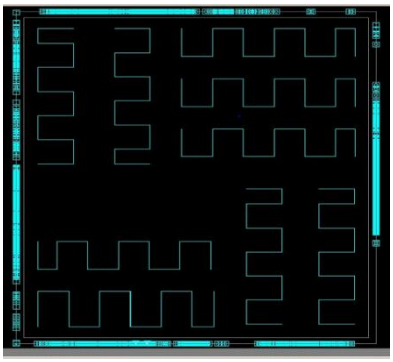


Fig. 5. Serpentine-Shaped Memory Macros Placed in the Floorplanning Stage

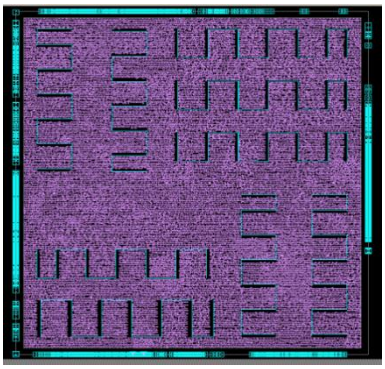


Fig. 6. Serpentine-Shaped Memory Macros Placed Above the Logic Cells [17]

After the global placement of the logic cells, the detailed placement stage was performed, involving the optimization of the logic cells and the interconnections between them. This is evident from the increase in the area occupied by the combinational logic cells and by the larger number of buffers and inverters used to meet the circuit timing constraints. This increase is less significant in the case of the 3D implementation due to the shorter distances between the memory macros and their associated logic.

The implementation of the 3D circuit up to this stage was achieved by modifying both the technology files and the scripts used in the implementation flow, with the modifications performed iteratively by adapting and refining the implementation methodology according to the obtained results; after placing the memory macros, represented by serpentine-shaped patterns, above the standard cells of the circuit, the "serpentine representations" were replaced with "ghost representations" (representations that allow the memory macros to completely overlap the standard logic cells), as shown in Figure 7, where the ghost memory representations replace the serpentine memory representations; the ghost representations could not be used from the beginning of the placement stage and therefore had to be preceded by the serpentine representations because the initial global placement step (create_placement) does not take into account the OVERLAP attribute used in the ghost representations, causing the placement tool to estimate an area utilization approaching 200%.

The replacement of the serpentine-shaped memory representations with ghost memory representations is performed only after the first placement stage of the implementation flow, while the replacement with the actual memory macros is carried out only at the end of the flow, immediately before the GDSII (Graphic Data System II) export.

The transition between the different stages of the implementation flow is performed using the virtual memory representations (serpentine and ghost) to avoid potential DRC violations (placement and routing violations) that would occur if the actual memory macros were used. Replacing the serpentine memory representations with ghost memory representations is necessary to make use of the area previously occupied by the serpentine patterns for timing optimization and, consequently, for a more efficient utilization of the available area. A placement optimization was then performed, rearranging the logic cells according to the timing and area constraints. Figure 8 illustrates the resulting rearrangement and automatic placement of the logic cells underneath the memory macros after optimization, as well as the filling of the space previously occupied by the serpentine memory representations.

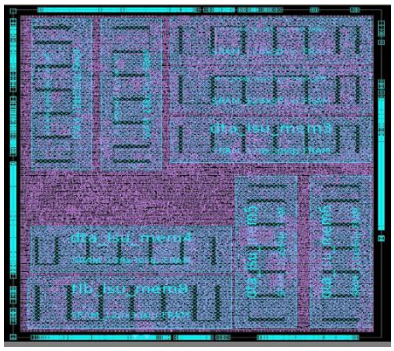


Fig. 7. Replacement of serpentine structures with phantom memory cells defined in the technology files

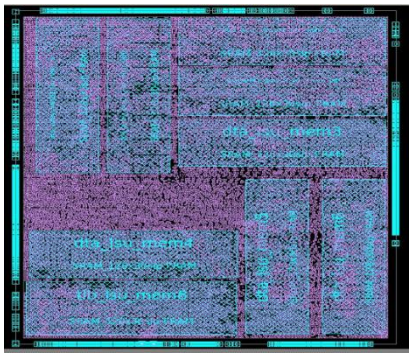


Fig. 8. Final placement of the memories above the standard cells.

The following section provides a detailed description of the preparatory stages and the implementation steps required to place the memory macros above the logic cells. In the conventional 2D planar design flow, the design tool operates in a single dimension, considering only the first layer of the circuit, and is therefore unable to perceive or incorporate the second layer.

The following subsections describe the methodology developed to overcome this technical limitation and implement a solution that enables the placement of memory macros within an area originally intended exclusively for logic cells, while complying with the constraints imposed by the specifications of the design tool.

Step 1: Circuit Evaluation

Before concluding that the most suitable circuit should consist of approximately half memory macros and half logic cells, several functional blocks of different sizes and occupying different areas were evaluated. However, the most suitable functional block for demonstrating the advantages of 3D integration over conventional 2D integration, using the methodology described previously, is one in which the memory macros occupy approximately half of the total area and

can be placed on Layer 2, while the logic cells occupy the remaining half of the area and are placed on Layer 1. Although the two layers serve different purposes, their utilization depends on the circuit size, the size of the memory macros, the number of memory macros, and the overall shape of the circuit. In the case presented in this work, a rectangular placement area for the logic cells was selected to accommodate the memory macros as efficiently as possible. In the general case of an integrated circuit implementation, however, the shape of the placement area depends on the design constraints. There are also minor exceptions to the 50% memory macros and 50% standard logic cells rule for the circuit implemented and analyzed in this work, which can be summarized as follows:

Exception 1: There are custom memory macros that allow abutment on three sides because all of their pins are located on a single side. Such memory macros allow abutment on all four sides in the 3D placement stage, which can result in an area utilization of up to 100% on Layer 2 [18].

Exception 2: Small memory macros may remain on Layer 1 together with the standard logic cells [18].

All circuit components, including the standard logic cells and the memory macros, are available in the following model formats: .lib (the library file containing the timing and power models of the components), .db (the compiled version of the .lib library), .LEF (the library file containing the physical representation of the components and their electrical parameters), and .MW (the Milkyway libraries generated by compiling the .LEF libraries together with the technology file (.tf) and the compiled .db libraries into a physical database visible to the physical design tool).

Since the memory macro pins on Metal 1 would create placement problems because all standard logic cells also have their pins on Metal 1, potentially leading to short circuits, all memory macro pins are relocated to Metal 7 (the implementation uses six metal layers). Consequently, Metal 7 can be considered the first metal layer of layer 2.

Considering the memory area and the area utilization on the second layer, as well as the area of the standard logic cells and the area utilization on layer 1, a reduction factor for the memory size can be calculated. Each memory must be reduced by this factor on each of the 4 sides; the width and the height of the memories are reduced by 2 multiplied by the reduction factor. This is due to the way in which the 2D tool from Synopsys evaluates the area of the whole circuit at the beginning of the memory block placement stage. The Synopsys 2D tool for evaluating and verifying the circuit area does not understand and does not know about the second layer and considers that the whole circuit is placed on the same layer; therefore an area utilization greater than 100% is not acceptable. The total area of the memory blocks should be equivalent to the area

of the standard logic cells (for example, a 90% utilization on the second layer leads to a reduction of the total area of the memory blocks with the area of the logic cells, considering a 100% utilization), minus 10% of the area on the second layer. This reduction of the memory size is necessary in order to allow the placement tool to optimize the placement; otherwise, in the situation where the memories would occupy 100%, the placement tool would have no placement options.

Step 2: Placement of the memory blocks

In this stage, the LEF technology files, which contain information about the physical shape of the memories and the positions of the pins, are updated with the new values of the memory block dimensions, obtained after reducing the dimensions on each side by the value calculated in the initial phase. Another update that appears in the LEF technology files is the "serpentine" shape, which is an obstruction having the shape of a "snake", which has a "meander pitch constant" smaller than the dimension (width and length) of the smallest memory on the second layer. In Figure 9, the "meander pitch constant" and the "snake" shape of a memory block have been highlighted. These updates in the LEF technology files, shape and dimension, together with the original .db files, are used to generate the new files using Milkyway from Synopsys, files that contain information about the new shapes of the memory blocks, files called "reduced serpentines".

In this way, a "HALO" is defined for each memory, which represents the free space (translated as a placement blockage for any kind of cell) left around the memories during automatic placement, and whose value is equal to 2 multiplied by the memory reduction factor plus the minimum distance between the memories (a minimum distance of 5 microns between memories was calculated). With this "HALO" width, one can pass the area verification stage carried out by the 2D area verification tool after the placement of the memory blocks. The reduction factor in the present situation is 15 microns; therefore the "HALO" has a value of 35 microns.

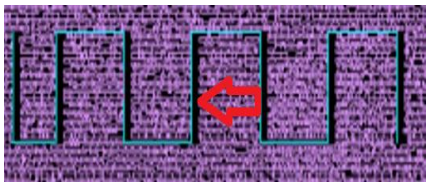


Fig. 9. Serpentine-Shaped Pattern and Meander Pitch

The tool that places all the memory blocks positions all the blocks without overlapping them, due to the "snake" shape, and without placing them too close to each other, due to the "HALO" requirement. The placement that results, taking into account these newly defined parameters, is done keeping a certain distance between the memory blocks, as well as between the memory blocks and the edge of the circuit, a distance whose value will later allow the memory

blocks to be expanded to their real shape without the memories overlapping each other inside the area needed for placing the memories.

Step 3: Detailed placement

In this stage, Milkyway files called "serpentines" are used, files that are generated using the original .db files and the .LEF technology files updated with the "snake" shape. The "serpentine" files used in this stage contain serpentine-shaped memories of non-reduced dimension; the "snake" is extended up to the edge of the real memory. To transmit the memory block placement information from stage 2 to stage 3, there are two ways: the first method is to copy the database from stage 2 and link it to the new Milkyway library, and the second method consists in saving the placement of the memory blocks in stage 2 and loading it in stage 3. The second method is more efficient, and once this method is carried out, the placement of the blocks is locked. The usual placement, similar to the placement in the 2D flow, follows after this phase. The integrated circuit design flow is continued and the clock tree is built in the 2 scenarios, 2D and 3D. The architecture of the clock tree is presented in the two integration scenarios: 2D (planar) and 3D (three-dimensional), and the reports generated after the implementation are analyzed. The purpose of this analysis is to compare the characteristics of each scenario and to highlight the advantages that three-dimensional integration can offer over the traditional 2D approach.

After the step of placing the circuit components, the implementation of the clock tree follows, with a view to obtaining an efficient skew, by inserting buffers and inverters on the clock signal paths. Clock tree synthesis is an important stage in the integrated circuit design flow and plays an important role in the implementation of a balanced clock tree that helps meet the timing constraints of the circuit. The main aim in building the clock tree is to reduce both the latency on the tree and the skew between the sequential components in the circuit, which are critical in terms of timing, and at the same time to keep the area of the circuit as small as possible.

In the first phase, the clock tree was implemented for the 2D integration of the circuit, and in Figure 10 the buffers and inverters that form the clock tree implemented for a period of 3 ns are highlighted by being marked in white. The structure of the clock tree in the 2D scenario comprises 8 levels with 274 buffers and inverters that reach the 7729 sequential cells in the circuit.

After placing the logic on layer 1 and the serpentine-shaped memory blocks on layer 2, the clock tree was implemented on layer 1 (Figure 11) in the 3D dimension, using the clock tree building tool embedded in ICC Synopsys. The library used in the implementation contains buffers and inverters of different sizes, starting from 0X up to 32X, where this X factor indicates a proportional scaling of the size of the internal transistors of the cell relative to a reference. The larger the X factor, the greater the drive strength of the logic cell, and thus that cell can drive larger

capacitive loads, reducing the signal delay on long wires and also reducing the power consumption. In the structure of the clock tree, buffers and inverters from the available technology were used, with sizes between 2X and 32X, in order to ensure a balanced tree with a minimized area. In the absence of the obvious area constraints from the 2D scenario, where all the components must be placed on a single layer, the distribution of the clock tree in the 3D configuration becomes much more uniform. This uniformity is due to the possibility of dispersing the nodes of the tree more efficiently over several levels, reducing the excessive concentration of resources in a single zone. A direct consequence of this optimized distribution is the significant decrease in the need for buffers and inverters. In the 3D architecture, the distances are reduced due to the layering of the components, allowing a more efficient propagation of the clock signal and, implicitly, reducing. the need to insert a large number of signal-regeneration elements.

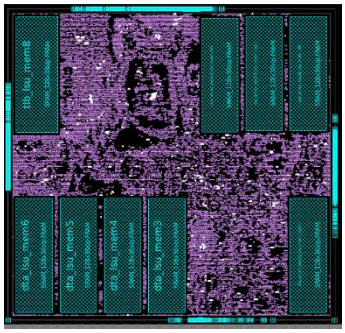


Fig. 10. Clock Tree Generated for the 2D Scenario [14]

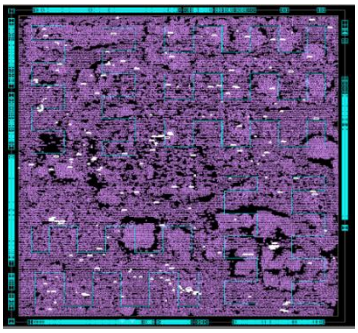


Fig. 11. Clock Tree Generated for the 3D Scenario [14]

The detailed report presented in Table 1 [14] compares the characteristics of the l2clk clock tree for both the 2D and 3D implementations. In both cases, the clock tree was synthesized for the functional scenario using a clock period of 3 ns and a circuit containing 7,729 flip-flops. The 2D implementation consists of 8 clock tree levels, 274 clock tree buffers with a total area of 1565.27 μm^2, and 464 clock cells occupying a total area of 2057.03 μm^2, while the maximum global skew is 0.056 ns. In comparison, the 3D implementation consists of 9 clock tree levels, 204 clock tree buffers with a total area of 1383.56 μm^2, and 393 clock cells occupying a total area of 1879.39 μm^2, with a maximum global skew of 0.046 ns.

As shown in Table 1, the 3D implementation reduces the number of clock tree buffers by 25.55%, the total number of clock cells by 15.30%, the total area of the clock tree buffers by 11.61%, the total area of the clock tree cells by 8.64%, and the maximum global skew by 17.40% compared with the conventional 2D implementation. These results demonstrate the advantages of three-dimensional integration by reducing the clock distribution resources while improving the overall clock tree performance.

Table 1. Comparison of Clock Tree Synthesis (CTS) Results for 2D and 3D Implementations

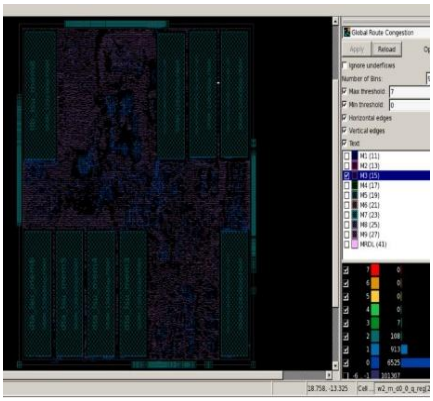
Parameter	CTS 2D	CTS 3D	Variation (3D vs. 2D) (%)
Clock Tree Name	l2clk	l2clk	-
Scenario:	func	func	-
Clock Period:	3.00000	3.00000	-
Clock Tree root pin	l2clk	l2clk	-
Number of Levels	8	9	**−12.50**
Number of Sinks	7729	7729	**0.00**
Number of CT Buffers	274	204	**25.55**
Number of CTS added gates	0	0	**0.00**
Number of Preexisting Gates	180	180	**0.00**
Number of Preexisting Buf/Inv	10	9	**10.00**
Total Number of Clock Cells	464	393	**15.30**
Total Area of CT Buffers (µm²)	1565.273	1383.560	**11.61**
Total Area of CT cells (µm²)	2057.038	1879.392	**8.64**
Max Global Skew (ns)	0.05655	0.04670	**17.40**

The three-dimensional optimization of the circuit reduces the connection lengths, both the average and the maximum ones, needed to connect the components of the circuit, reducing the power dissipation and increasing the performance at the same time. The total reduction of the circuit area, due to the stacking of the memory blocks over the standard cells, is reflected at the level of the clock tree in the following aspects:

- ✓ The total number of clock cells was reduced by 15.3%;
- ✓ The number of inverters and buffers used to create the clock tree decreased by 25.5%;
- ✓ The skew value is reduced by 17.8%.

After the implementation of the clock tree, the routing of the circuit was carried out, a stage in which the logical connections between the components of the circuit are also physically implemented with the metals from the technology. The technology used for implementing this circuit contains 10 metals, from M1 to RDL (ReDistribution Layer), the RDL being the TOP metal, generally made of aluminum. For the routing of the signal connections, only 6 metals out of 10 were used for the first layer, the last ones being used for the routing on the second layer, where M7 becomes the first routing metal - on M7 are the pins of the memories on the second layer. An important factor in the routing stage is the congestion on each metal, which is the ratio between the number of available routing tracks and the number of routing tracks needed to route the connections. In Figures 12 and 13 are presented screenshots taken within the ICC Synopsys design

environment, and they represent the routing congestions on metal 3 in the 2 integrated circuit design scenarios: 2D and, respectively, 3D.



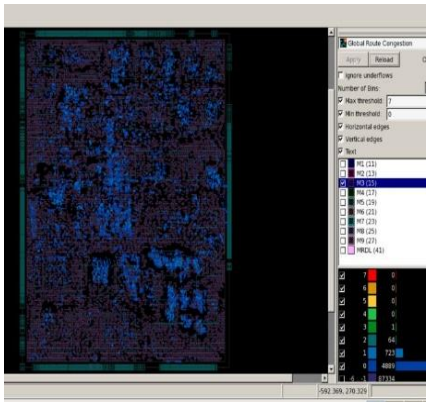


Fig. 12. Congestion on M3 after 2D routing Fig. 13. Congestion on M3 after 3D routing

The congestion at the level of the Metal 3 layer in the 2 scenarios, 2D and 3D, is highlighted by the blue color, which, as can be seen, is more accentuated and more compact in the 3D scenario, due to the reduction of the area over which the integrated circuit is implemented. This increase in the congestion on metal 3 is a direct consequence of the reduction of the total area available for routing, a result of the stacking of the memory blocks over the standard logic cells. Due to the vertical integration over the two layers, the total area of the circuit is minimized and the density of the metals during routing is concentrated in a more compact space, thus avoiding the waste of unused silicon area

A high congestion on each metal, as can be seen in Figure 13, highlights an optimal use of the circuit area and a more efficient routing of the interconnections than in the 2D scenario. In the report in Table 2, information is extracted about the total number of connections in the circuit, about the length of the metals used for routing the signal interconnections and the number of contacts used between the metals, reports generated after the detailed routing stage. The length of the routed connections is reported for each metal, from M1 up to M6. The total length of the routable connections in the 3D scenario decreases by approximately 16% compared with the 2D scenario.

One can observe the decrease in the total length of the interconnections in the case of 3D placement and routing, as well as the decrease in the length on each metal compared with 2D placement and routing. Also, the number of contacts used for moving from one metal to another is smaller in the case of 3D placement and routing. Compared with the 2D implementation, 3D integration allows a more efficient distribution of the cells over multiple layers, which leads to a reduction of the total area occupied by the circuit.

Table 2. Routing Report: 2D vs. 3D Implementation

Parameter	2D Routing	3D Routing	Variation (%)
Total Wire Length (µm)	1413384	**1185951**	**16.09**
Total Number of Contacts	296263	**282697**	**4.58**
Total Number of Wires	296115	**280907**	**5.14**
Total Number of PtPConns	43717	**42127**	**3.64**
Total Routable Wires	296115	**280907**	**5.14**
Total Routable Wire Length (µm)	1413384	**1185951**	**16.09**
M1 Wire Length (µm)	132506	**91947**	**30.61**
M2 Wire Length (µm)	459813	**379519**	**17.46**
M3 Wire Length (µm)	367047	**345682**	**5.82**
M4 Wire Length (µm)	206906	**157387**	**23.93**
M5 Wire Length (µm)	141079	**127957**	**9.30**
M6 Wire Length (µm)	106032	**83458**	**21.29**

Chapter 5 introduces the idea of modeling 3D neuromorphic structures that would be capable of locally processing AI (Artificial Intelligence) algorithms with a minimum energy consumption and occupying a minimum space. An element of novelty is the launch and presentation of the concept of the "Neural Grain", which is a hardware AI structure that mimics a structure of the biological brain [19]. A 3D cubic structure of a "Neural Grain" was modeled, and a VHDL code was developed that is implemented, through the VIVADO synthesis tool, in an FPGA circuit from the ARTIX 7 family. In parallel, the same NG 4x4x1 structure was modeled in a technology that emulates monolithic 3D technology, by going through the synthesis steps using the Genus tool from Cadence.

The VHDL module, named neuron_NG, models a single artificial neuron (perceptron) using digital logic. It takes two inputs—an 8-bit input value \(x_i\) and an 8-bit bias—and produces a binary output signal \(Y_o\) based on a comparison between the two inputs. The schematic generated after implementing the VHDL code on the FPGA board is shown in Fig. 13. It consists of three vertically arranged neuron layers, with the first two layers containing four neurons each and the final layer containing a single neuron. As illustrated in Fig. 13, each neuron in the network consists of a multiplier and a memory cell.

The Neural Grain network is introduced as a novel modular 3D neural architecture, defined as a compact 4×4×1 multilayer perceptron that can serve as an atomic computational unit within larger, scalable neural systems.

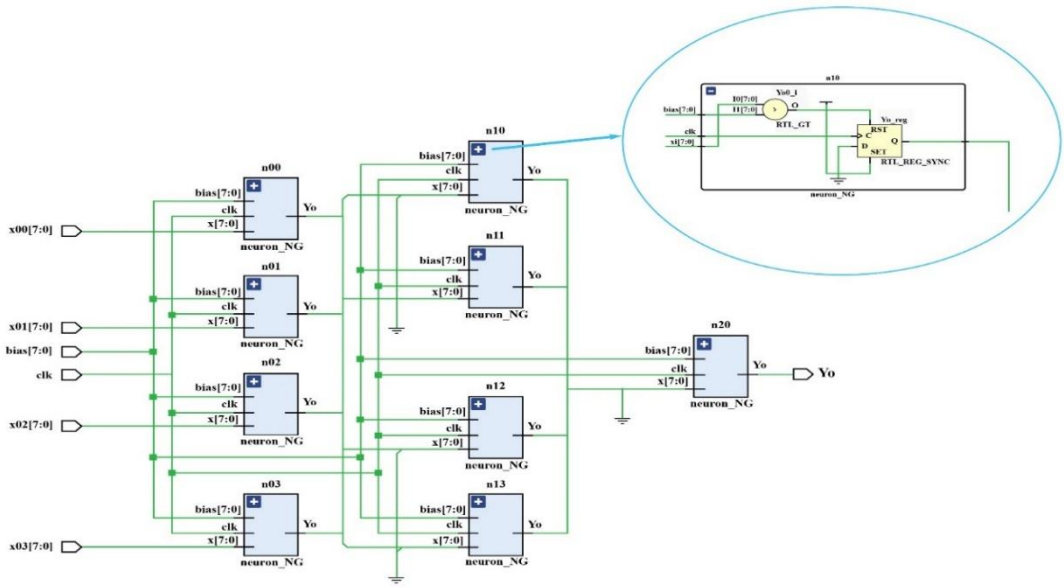


Fig. 13 Schema generată cu instrumentul VIVADO pentru rețeaua Grain

Unlike traditional neural network architectures, which typically adopt layer-centric 2D topologies with globally distributed weights, Neural Grain emphasizes physical modularity, local computation, and hardware-optimized circuitry. It enables straightforward replication and arrangement on FPGA-based platforms or neuromorphic systems without requiring the redesign of routing logic or resource allocation. While traditional neural architectures, such as fully connected networks (FCNs), convolutional neural networks (CNNs), and recurrent neural networks (RNNs), offer topological flexibility and high performance in software and cloud environments, their hardware implementations are often constrained by scalability issues, real-time requirements, and high energy consumption. In contrast, Neural Grain is particularly well suited for embedded systems and edge-AI applications, offering low-latency inference, deterministic behavior, and a reduced memory footprint. However, these advantages come at the cost of a more rigid structure and the lack of inherent support for spatial operations, such as convolution, making Neural Grain best suited as a building block for more complex hybrid architectures. Thus, the Neural Grain concept bridges the gap between abstract neural computation and practical, modular hardware implementations.

GENERAL CONCLUSIONS AND RECOMMENDATIONS

The topic proposed for research had as its aim the development of a methodology for implementing a three-dimensional circuit using the traditional 2D implementation tools, by adapting the technology files so that the stacking of the layers is allowed. This methodology offers support to monolithic 3D technology for fabrication, before the development of design tools that would support the multi-layer concept. Based on the research and the results obtained, the following general conclusions can be formulated:

1. The three-dimensional approach to implementing electronic circuits facilitates heterogeneous integration (the digital part, sensors and memories can be implemented on the same silicon die) and the use of mixed technologies (old technologies - 28nm - alongside new technologies - 7nm -, analog technologies - BiCMOS - alongside standard digital technologies - CMOS - and memory-specific technologies - FLASH) [10].

2. The described methodology creates a link between the theoretical principles and the best practices from industry, by integrating the real-world constraints, the tool limitations and the manufacturability considerations. This ensures that the flow is not only academically rigorous, but can be implemented in commercial semiconductor design environments, increasing its impact and applicability [17].

3. The working procedure used facilitates early-stage design space exploration, allowing designers to make informed trade-offs between power, performance and area. By efficiently structuring the synthesis, placement and routing strategies, it allows optimizations that ensure design efficiency, while respecting the timing, power and physical implementation constraints [15,17].

4. The use of TCL scripts facilitates the structured control of the iterations, allowing rapid adjustments and optimizations during synthesis, DFT, and placement and routing. This approach accelerates the convergence of the circuit and improves productivity by allowing efficient tuning of the parameters [17].

5. The monolithic 3D integration of the logic and the memories, achieved by adapting the 2D flow, led to a reduction of the total area by 50%. The total length of the routed connections decreased by approximately 20% in the 3D scenario compared with 2D. This reduction of the interconnection length led to a decrease of 13.5% in the total number of buffers**,** , due to the reduced need to compensate for the propagation delays on shorter wires [13].

6. The data propagation speed increases: designing the circuit using monolithic 3D technology leads to an increase in the performance of the final integrated circuit. The uniform

distribution of the clock network in the 3D scenario over the entire area of the circuit (due to the freeing up of area) compared with the 2D scenario led to [14]:

- ✓ The number of inverters and buffers used to create the clock tree decreased by 25.5%;
- ✓ The total number of clock cells was reduced by 15.3%;
- ✓ The total area of the inverters and buffers decreased by 11.6%;
- ✓ The total area of the clock cells was reduced by 9%;
- ✓ The number of levels of the clock tree increased by 12.5%, contributing to a more uniform distribution of the clock signal;
- ✓ The skew value is reduced by 17.8%.

7. In the development of the programs that would carry out the implementation of three-dimensional circuits, special attention will be paid to designing an efficient partitioning tool which, based on input data such as the netlist, the constraints file and the technology libraries, would generate solutions for dividing the circuit over the layers [18].

8. The structured and modular nature of the described working process lays the foundations for future progress in integrated circuit design. Potential areas for further research include the integration of artificial intelligence (AI) and machine learning (ML) techniques to improve synthesis and place-and-route optimizations, improvements in parallel processing methodologies, and further refinement of the verification strategies in order to increase automation and accuracy in early-stage circuit validation [17,19].

9. The transition from the methodology for designing integrated circuits in 2D technology to design in 3D technology represents a major challenge in microelectronics, but also an opportunity for innovation. The use of an experimental 3D design flow that uses 2D tools can serve as a starting point for adapting and developing new technologies that would facilitate progress in the development of three-dimensional integrated circuits. The entire Backend flow of the three-dimensional integrated circuit implementation was executed using standard 2D EDA tools, with appropriate modifications of the technology files [15,17].

Based on the analysis of the results obtained in the work, the following **recommendations can be formulated:**

1. It is recommended to use the tool chains accredited by the foundry whose process is used (e.g. TSMC uses tools from Synopsys and from Cadence) for the development and implementation of the flow and/or of the three-dimensional integrated circuit.

2. It is recommended to understand in depth the technology files (LEF, DEF, LIB) that are to be adapted for three-dimensional integration. The information contained in these files can be

modified so as to facilitate the acceptance, by the placement and routing tools, of the overlapping of the cells with each other without reporting errors.

3. Understanding in detail the way the tools used for implementing the flow work - with reference to the internal algorithms, the stages in which they are used and the sequence of these stages. This is recommended in order to understand the way the tools interpret the input data in each stage and the way the parameters specific to each stage are evaluated.

4. It is recommended to use circuits that lend themselves to the three-dimensional approach - they present advantages when using different technologies:

a. they require analog components (e.g. converters, PLL);

b. they use FLASH memories;

c. they contain a need for SRAM memories whose area is comparable to the area of the standard logic cells;

d. they contain functional blocks with a frequency requirement that can be implemented both in new technologies (e.g. CPU) and in older technologies (e.g. communication interface).

5. Before investing in 3D placement and routing tools, it is recommended to carry out research and analysis on the circuit and the library with the help of the current 2D tools. In this way, the advantages of the three-dimensional implementation can be validated in terms of area, connections, speed and power consumption, and the flow to be used with the 3D tools can be developed.

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LIST OF PUBLICATIONS RELATED TO THE THESIS

by Pletea Ionica-Marcela, PhD candidate (part-time doctoral studies),
Specialty 233.01 – Nano-Microelectronics and Optoelectronics

List of Publications Related to the Thesis

Articles published in the proceedings of scientific conferences indexed in Web of Science and Scopus:

1. **Pletea, I.M.**, Wurman Zeev, Or-Bach Zvi, Şontea Victor. Monolithic 3D layout using 2D EDA for embedded memory-rich designs. În: *IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference S3S 2015*. 2015. New Jersey. p. 1-2. ISBN 978-150900259-7.
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4. **Pletea, I.M.**, Şontea Victor, Cojocaru Victor. Impactul conexiunilor verticale asupra ariei in integrarea 3D. În: *Conferința Internațională* "*Telecommunicații, Electronică și Informatică".* Ed. 6. 2018. Chișinău, Republica Moldova. pp. 375-377. ISBN 978-9975-45-540-4.
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6. **Pletea, I.M.**, Şontea Victor. Design and Partitioning Across 2 Strata în 3D IC architectures. În: *International Conference on Electronics, Communications and Computing*,

IC ECCO 2024. Editia 13. 2024. Chișinău. Pp. 107-108. ISBN (pdf) 978-9975-64-480-8 (PDF).

Articles published in the proceedings of scientific conferences listed in the Register of publications from scientific conferences organized in the Republic of Moldova:

7. **Pletea, I.M**., Impactul integrării 3D asupra Construirii Arborelui de Clock. În: *Conferinţa tehnico-ştiinţifică a studenţilor, masteranzilor şi doctoranzilor*. Vol.1. 2019. Chișinău, Republica Moldova. Vol. 1, pp. 397-399. ISBN 978-9975-45-588-6.
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Articles published in journals listed in the National Register (Category Indicated):

9. **Pletea, I.M**., Methodology and backend flow optimization for 3D. În: *Journal of Engineering Science,* categoria B+. 2024, Vol. 31 Nr. 2 (iulie 2024), pp. 39–47. ISSN 2587-3474.

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11. **Pletea I.M**., Arhitectura 3D monolitică hibridă. Cerere de brevet de invenție Numărul A2025/00521 din 12.11.2025.
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ANNOTATION

to the thesis entitled "DESIGN OF VERTICAL INTEGRATED CIRCUITS USING CURRENT 2D DIGITAL DESIGN SOFTWARE", submitted by PLETEA Ionica-Marcela, for the award of the scientific degree of Doctor of Engineering Sciences, in the specialty 233.01 "NANO-MICROELECTRONICS AND OPTOELECTRONICS"

Thesis structure: The thesis is written in Romanian and consists of an introduction, 5 chapters, general conclusions and recommendations, a bibliography of 141 titles, 7 annexes, 113 pages of basic text, 61 figures, 5 tables. The results obtained are published in 10 scientific articles and validated through 2 implementation certificates and 2 patent applications filed, which attest to the practical applicability of the methodology and solutions developed within the doctoral research

Keywords: integrated circuits, nanotechnologies, vertical integration, monolithic 3D, EDA

The purpose of the work: consists of developing an integrated methodology for the design and experimental validation of 3D monolithic circuits, with a focus on adapting the workflow, technological files, and traditional 2D implementation tools, to vertical integration.

Research objectives: The research objectives included the development of a key method required for adapting 2D EDA tools to the design of integrated circuits using monolithic 3D integration technology. To achieve this goal, a methodology was developed based largely on existing 2D integrated circuit design flows, complemented by specific steps required for monolithic 3D integration. The research focused on modifying the floorplanning, placement, and routing stages to make them aware of the third dimension. In addition, the libraries used throughout the design flow were extended with parameters, attributes, and values specific to monolithic 3D integration. Another objective was the definition of a two-tier partitioning strategy, where logic cells are placed on the first tier and memory blocks on the second tier, enabling the efficient application of the proposed methodology.

Scientific novelty and originality: consists in the demonstration of the implementation of a 3D monolithic integrated circuit using only 2D design tools. The approach proposed in this thesis is to reuse as much as possible existing conventional 2D EDA tools and focus only on a few critical EDA elements necessary to enable the creation of efficient 3D methodologies using current tools.

The scientific and research problem solved: consists in developing this methodology that allows 2D EDA tools to design monolithic 3D integrated circuits. This 3D design methodology using 2D tools will help chip manufacturers manufacture better performing and smaller chips at the same cost using existing and already depreciated manufacturing equipment.

Theoretical significance and applied value of the work: The proposed methodology provides the foundation for the development of a complete design process for integrated circuits using monolithic 3D technology. The application of this methodology creates the prerequisites for the realization of integrated circuits with enhanced performance and reduced power consumption while leveraging existing infrastructure and contributing to lower development costs.

Implementation of scientific results: The research results demonstrate the feasibility of using 2D design tools for the implementation of monolithic 3D integrated circuits and validate the practical applicability of the proposed methodology. These results will be transferred to the educational environment through the development and introduction of a course module dedicated to 3D integrated circuit design for master's students, contributing to the training of specialists in advanced microelectronics.

PLETEA IONICA-MARCELA

DESIGN OF VERTICALLY INTEGRATED CIRCUITS USING CURRENT 2D DIGITAL DESIGN SOFTWARE

233.01 ” NANO-MICROELECTRONICS AND OPTOELECTRONICS”

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